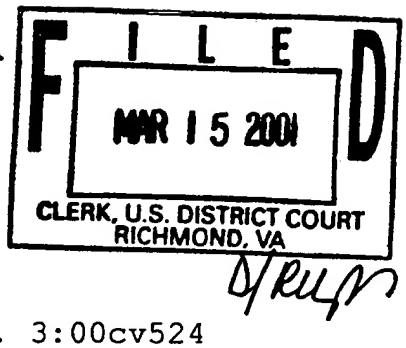
IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF VIRGINIA
Richmond Division



RAMBUS, INC.,

Plaintiff,

v. Civil Action No. 3:00cv524

INFINEON TECHNOLOGIES AG
and INFINEON TECHNOLOGIES
NORTH AMERICA CORP.,

Defendants.

MEMORANDUM OPINION

This action involves four patents and fifty-seven claims. All four patents in suit descend from a common progenitor, the specification of which controls the patents in suit. The parties are in agreement that construction of the claims here at issue is confined to construction of eight disputed terms ("bus," "block size," "read request," "write request," "transaction request," "first external clock signal," "second external clock signal" and "integrated circuit device") each of which, with but one exception,[1] has the same meaning in each claim in issue in all four patents in suit. Hence, the agreed upon scope of claim construction is to construe the eight terms.

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[1] The parties agree that all the terms have the same meaning throughout with the exception of "integrated circuit device." The Defendants contend that this term has a different meaning in one patent due to representations made to the Patent and Trademark Office during the prosecution of that patent.

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The parties have briefed the issues, have presented evidence at a hearing conducted pursuant to the requirements of Markman v. Westview Instruments, Inc., 517 U.S. 370 (1996), and have argued orally. Against this background, the eight disputed terms, and hence the claims, are accorded the constructions set forth below.

BACKGROUND

In 1990, the co-founders of Rambus, Inc. ("Rambus"), Mark Horowitz and Paul Michael Farmwald, filed a patent application describing numerous inventions designed to increase the operating speed of memory devices in computers. The Patent Office determined that this application, U.S. Patent App. No. 07/510,898 ("the '898 application"), actually contained 11 independent and distinct inventions, required Rambus to select only one of those inventions to pursue in the '898 application, and allowed Rambus to file divisional applications on the remaining inventions described in the '898 application. Rambus did precisely that, electing to pursue one invention within the '898 application and thereafter filing ten more applications in the next six months. Subsequently, continuation and divisional applications were filed on these ten applications; and thus, to date, Rambus has been granted 31 patents based on the 1990 '898 application. Numerous applications are currently pending.

By way of background, the patented inventions have to do with computer memory devices called Dynamic Random Access Memory

("DRAM") and a system and devices for increasing the speed at which data or information is transferred between the DRAM and the Central Processing Unit ("CPU") of a computer. The DRAM is a high-speed, short-term memory device where information being used by the CPU is stored. The patents in suit describe numerous inventions respecting the memory interface and a new type of "bus" which carries information or data. The "Field of Invention" section of the specification, common to all patents in suit, gives the following overview of the inventions:

> [a]n integrated circuit bus interface for computer and video systems is described which allows high speed transfer of blocks of data, particularly to and from memory devices, with reduced power consumption and increased system reliability. A new method of physically implementing the bus architecture is also described.

U.S. Patent No. 6,034,918 (issued March 7, 2000) ("the '918 patent"), col. 1, ll. 20-25.[2]

On August 8, 2000, Rambus instituted this action for the infringement of four of its patents against Infineon Technologies AG (a German corporation), Infineon Technologies, Inc. (a German corporation) Infineon Technologies North America Corp. (a Delaware corporation) and Infineon Technologies Holding North America, Corp. (a Delaware corporation) (collectively referred to as "Infineon").

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[2] All the patents in suit, and all the patents springing from the 1990 '898 application, contain the same specification. For ease of citation, all references to the specification will be to the '918 patent.

The first of the patents in suit, U.S. Patent No. 5,953,263 (issued Sept. 14, 1999) ("the '263 patent"), claims a latency invention which involves the use of a programmable register on the DRAM chip to store a value representative of a time delay. The latency invention makes the DRAM response time more predictable because the CPU knows precisely when it will receive data from the DRAM in response to a transaction request, thereby allowing the system to plan for transfers and improving overall traffic flow over the bus.[3] Claims 1-5, 14, 16-19, 21, 23-25, 27-28, 30 and 32-33 of the '263 patent are at issue in this action.

Secondly, in U.S. Patent No. 5,954,804 (issued Sept. 21, 1999) ("the '804 patent"), Rambus claims a delayed lock loop (DLL) on a DRAM chip, which allows precise timing of the output of data. In essence, the DLL allows the DRAM chip to collect the data from the memory cells and then paces the release of that information over the bus. The DLL becomes useful when operating the DRAM at high

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[3] Claim 1 of the '263 patent is representative of this invention:

> 1. A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
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> a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request.

rates of speed.[4] Claim 26 of the '804 patent is the only claim involving this invention at issue in this action.

The third patent, U.S. Patent No. 6,034,918 (issued Mar. 7, 2000) ("the '918 patent"), covers the variable block size invention, which involves the use of circuitry to allow for the output of variable-sized blocks of data over the bus in response to a transaction request. The additional circuitry allows a user, such as a CPU, to select differing sizes or blocks of data, instead

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[4] Claim 26 of the '804 patent describes DLL in combination with the latency invention:

> 26. An integrated circuit device having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device outputs data on an external bus synchronously with respect to first and second external clock signals, the integrated circuit device comprises:
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> a first internal register to store a value which is representative of a number of clock cycles to transpire before the integrated circuit device responds to a read request;
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> delay locked loop circuitry to generate an internal clock signal using the first and second external clock signals; and
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> interface circuitry, coupled to the external bus to receive a read request, the interface circuitry includes a plurality of output drivers, coupled to the external bus, to output data on the external bus in response to the internal clock signal, synchronously with respect to the first and second external clock signals and in accordance with the value stored in the first internal register.

of a single piece of data.[5] Claims 1-2, 6, 8-9, 13, 15-20, 24-25, 29-31, 33 and 34 of the '918 patent are at issue in this action.

Lastly, U.S. Patent No. 6,032,214 (issued Feb. 29, 2000) ("the '214 patent") claims double data rate ("DDR") as the invention. In general, memory devices send and receive information according to a clock contained within the computer system. Clocks are a common, but important, feature of all computer systems. Before the DDR invention, information was transferred only on the "tick" of the clock. The memory device using that type of transfer regulator is called a Synchronous DRAM, or "SDRAM." The DDR invention allows information from the SDRAM to be sent out on both the "tick" and

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[5] Claim 18 of the '918 patent describes this invention as:

> 18. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:
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> receiving an external clock signal;
>
> receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request;
>
> receiving a first request from the bus controller; and
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> outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal.

the "tock" (or the rising and falling edges) of the computer's internal clock, thereby doubling the data output of the SDRAM for a given clock rate.[6] Claims 1-2, 4, 6, 9-11, 14-16, 18-19, 21, 24-26 and 29 of the '214 patent are at issue in this action.

Infineon makes, uses, sells or offers to sell, and imports SDRAM devices, DDR SDRAM devices and Synchronous Graphics RAM ("SGRAM") devices, as well as products, such as computers, servers, automated teller machines, telephones and telephone systems and point of sale terminals, all of which contain SDRAM, DDR SDRAM or

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[6] Claim 15 of the '214, which is representative of this invention, covers this invention in combination with the variable block size described in the '918 patent:

> A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method comprising:
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> receiving first block size information, wherein the first block size information defines a first amount of data to be output onto a bus in response to a read request;
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> receiving a first read request; and
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> outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to a first and a second external clock signal wherein a first portion of the first amount of data is output synchronously with respect to the first external clock signal and a second portion of the first amount of data is output synchronously with respect to the second external clock signal.

SGRAM devices. Rambus alleges that all of those devices and the products and modules into which they are incorporated infringe some or all of the patents in suit. Infineon denies that its products infringe any of those patents.

DISCUSSION

I. The Legal Standard

Patent infringement analysis involves two steps: ascertaining the proper construction of the patent claim and determining whether the accused method or product infringes the properly construed claim. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). A patent contains two distinct elements: "First, it contains a specification describing the invention 'in such full, clear, concise and exact terms as to enable any person skilled in the art . . . to make and use the same.' 35 U.S.C. § 112 . . . . Second, a patent includes one or more 'claims,' which 'particularly poin[t] out and distinctly clai[m] the subject matter which the applicant regards as his invention." Markman v. Westview Instr., Inc., 517 U.S. 370, 373 (1996).

The construction or interpretation of a claim is a question of law. Markman v. Westview, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), aff'd 517 U.S. 370 (1996). "[I]n interpreting an asserted claim, the court should look first to the intrinsic evidence of record, i.e., the patent itself, including the claims, the

specification and, if in evidence, the prosecution history. Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." Vitronics, 90 F.3d at 1582 (internal citations omitted). If the intrinsic evidence is insufficient to resolve ambiguity in the meaning of claims, the court may rely upon extrinsic evidence to understand the technology and to construe the claims. Id. at 1584. "Extrinsic evidence is that evidence which is external to the patent and file history, such as expert testimony, inventor testimony, dictionaries, and technical treatises and articles." Id. Extrinsic evidence, however, may not be used to contradict the claim language or the meanings established in the specification. Id. "Any other rule would be unfair to competitors who must be able to rely on the patent documents themselves, without consideration of expert opinion that then does not even exist, in ascertaining the scope of a patentee's right to exclude." Id. (quoting Southwall Tech. Inc. v. Cardinal IG Co., 54 F.3d 1570, 1578 (Fed. Cir. 1995), cert. denied, 516 U.S. 987 (1995)).

In the examination of the intrinsic evidence, "there is a hierarchy of analytical tools. The actual words of the claim are the controlling focus." Digital Biometrics, Inc. v. Identix, Inc., 149 F.3d 1335, 1344 (Fed. Cir. 1998). Thus, a court should first "look to the words of the claims themselves, both asserted and nonasserted, to define the scope of the patented invention."

Vitronics, 90 F.3d at 1582. See Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305 (Fed. Cir. 1999) ("The starting point for any claim construction must be the claims themselves."); K-2 Corp. v. Salomon S. A., 191 F.3d 1356, 1362 (Fed. Cir. 1999) ("We begin, of course, with the language of the claims").

"The general rule is that terms in the claim are to be given their ordinary and accustomed meaning." Id. See also Vitronics, 90 F.3d at 1582. "It is the person of ordinary skill in the field of the invention through whose eyes the claims are construed. Such person is deemed to read the words used in the patent documents with an understanding of their meaning in the field, and to have knowledge of any special meaning and usage in the field." Multiform Desiccants, Inc v. Medzam, Ltd., 133 F.3d 1473, 1477 (Fed. Cir. 1998). Notwithstanding that terms in the claim and specification are presumed to carry the ordinary meaning that they would have to one of ordinary skill in the field, "a patentee may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the special definition of the term is clearly stated in the patent specification or file history." Vitronics, 90 F.3d at 1582. See also Hoescht Celanese Corp. v. BP Chems. Ltd., 78 F.3d 1575, 1578 (Fed. Cir. 1996), cert. denied 519 U.S. 911 (1996) ("A technical term used in a patent document is interpreted as having the meaning that it would be given by persons experienced in the field of the invention, unless

it is apparent from the patent and the prosecution history that the inventor used the term with a different meaning").

> That is, the ordinary and accustomed meaning of a disputed claim term is presumed to be the correct one, subject to the following. First, a different meaning clearly and deliberately set forth in the intrinsic materials -- the written description or the prosecution history -- will control. Second, if the ordinary and

1997), cert. denied 522 U.S. 1109 (1998) (same). See also Toro Co. v. White Consolidated Indus., Inc., 199 F.3d 1295, 1299 (Fed. Cir. 1999) ("words of ordinary usage must nonetheless be construed in the context of the patent documents").

> The specification acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication. . . . The specification contains a written description of the invention which must be clear and complete enough to enable those of ordinary skill in the art to make and use it. Thus, the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.

Vitronics, 90 F.3d at 1582 (emphasis added). The ordinary meaning of claim terms is a "heavy presumption" to be overcome. Johnson Worldwide, 175 F.3d at 989.

As the third category of intrinsic evidence, "the court may also consider the prosecution history of the patent, if in evidence. This history contains the complete record of all the proceedings before the Patent and Trademark Office ["PTO"], including any express representations made by the applicant regarding the scope of the claims." Vitronics, 90 F.3d at 1583 (internal citations omitted). "[A]rguments made during prosecution regarding the meaning of a claim term are relevant to the interpretation of that term in every claim of the patent absent some clear indication to the contrary." Southwall Tech., 54 F.3d at 1579. "The prosecution history limits the interpretation of

claim terms so as to exclude any interpretation that was disclaimed during prosecution." Id. at 1576. "Claims cannot be construed in one way to obtain their allowance and in a different way against accused infringers." Id. See Digital Biometrics, 149 F.3d at 1344 ("The prosecution history is relevant because it may contain contemporaneous exchanges between the patent applicant and the PTO about what the claims mean").

When consideration of these three sources resolves the disputes over the asserted claim terms (as it generally should), reliance on extrinsic evidence to construe the claim is improper. Vitronics, 90 F.3d at 1583. This is because the claims, specification and file history comprise the public record of the patentee's claim, and to allow the public record (upon which competitors are entitled to rely when investigating the scope of the patentee's claimed invention), to be altered or changed by extrinsic evidence is to undermine the notice function of the public record. Id.

The preference for intrinsic evidence, however, does not preclude a court from considering or relying upon extrinsic evidence:

> Vitronics does not prohibit courts from examining extrinsic evidence, even when the patent document is itself clear. . . . Moreover, Vitronics does not set forth any rules regarding the admissibility of expert testimony into evidence. . . . Rather, Vitronics merely warned courts not to rely on extrinsic evidence in claim construction to

> contradict the meaning of claims discernible from thoughtful examination of the claims, the written description, and the prosecution history--the intrinsic evidence.

Pitney Bowes, 182 F.3d at 1308 (emphasis in original). See also Bell & Howell Document Mngmt. Prods. Co. v. Altek Sys., 132 F.3d 701, 706 (Fed. Cir. 1997) ("Use of expert testimony to explain an invention may be useful. But reliance on extrinsic evidence to interpret claims is proper only when the claim language remains genuinely ambiguous after consideration of the intrinsic evidence. . . .").

> This is especially the case with respect to technical terms, as opposed to non-technical terms in general usage or terms of art in the claim-drafting art. . . . Indeed, a patent is both a technical and a legal document. While a judge is well-equipped to interpret the legal aspects of the document, he or she must also interpret the technical aspects of the document, and indeed its overall meaning, from the vantage point of one skilled in the art.

Pitney Bowes, 182 F.3d at 1309.

Within the category of extrinsic evidence, some types of evidence are preferred over others: "prior art documents and dictionaries, . . . are more objective and reliable guides [than expert testimony]. Unlike expert testimony, these sources are accessible to the public in advance of litigation. . . . Indeed, opinion testimony on claim construction should be treated with the utmost caution, for it is no better than opinion testimony on the meaning of statutory terms." Id. at 1585.

These fundamental precepts inform and guide the construction of the claims at issue in this action. As mentioned previously, there are 57 different claims being asserted under the four patents in suit and each of those claims are in dispute and therefore must be construed. However, in their claim construction briefs the parties have circumscribed that rather daunting task by identifying eight terms to be interpreted. At the Markman hearing, the parties agreed that (with a previously noted exception) these eight terms have the same meaning in each of the 57 asserted claims. As a result, the claim construction task in this action reduces to construing the eight disputed terms. That task is undertaken *seriatim*.

II. Claim Construction

A. "Bus"

The parties dispute the meaning of "bus" as that term is used throughout the claims of the patents in suit. Rambus argues that "bus" means any "set of signal lines (for example, wires) to which a number of devices are connected, and over which information is transferred between devices." According to Rambus, "the term "bus" is old and very common in the electrical arts" and, in the patents in suit, the term is used in its ordinary and customary sense "as a set of signal lines over which information is transferred."[7] To

[7] Plaintiff Rambus Inc.'s Markman Brief Concerning Claim Construction, p. 13.

support the contention that this is the ordinary and customary construction of the term "bus," as used in its patents, Rambus relies not upon intrinsic evidence but upon the extrinsic evidence of the *IEEE (Institute of Electrical and Electronics Engineers) Standard Dictionary of Electrical and Electronics Terms,* Fourth Ed., IEEE Inc., New York (1988), p. 116, to explain how one skilled in the art would understand the term. The IEEE Dictionary defines a bus as "a set of signal lines used by an interface system, to which a number of devices are connected, over which information is transferred between the devices." Id.[8]

Infineon, on the other hand, contends that "bus" actually has a specialized meaning conferred by the specification of the patents in suit, which describes and explains the bus and its use with the other inventions as the Rambus "multiplexed bus." Before the '898 application was filed in 1990, most buses generally had point-to-point interfaces wherein the CPU would communicate with different memory devices by different and separate lines. Furthermore, within each bus in the prior art, the lines would be dedicated to

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[8] Of course, a court cannot use an inconsistent dictionary definition to contradict the meaning derived from the intrinsic evidence, but such definition may be of some assistance to the court in interpreting technical terms. See Vanguard Prods. Corp. v. Parker Hannifin Corp., 234 F.3d 1370, 1372 (Fed. Cir. 2001) ("Although a dictionary definition may not enlarge the scope of a term when the specification and the prosecution history show that the inventor, or recognized usage in the field of the invention, have given the term a limited or specialized meaning, a dictionary is often useful to aid the court in determining the correct meaning to be ascribed to a term as it was used.")

carrying either data, address, control or device-select information. In the new inventive Rambus bus, a single bus is multiplexed so that the bus lines carry all the address, control, data and device-select information over a single bus. In Infineon's view, the use of the term "bus" throughout the claims is limited to the new inventive bus described in the specification.

1. The Claim Language

The analysis begins by first considering the claim language.[9] Most of the 57 claims at issue use the term "a bus" or "the bus" or "an external bus." None of the claims, however, expressly define the term "bus," nor do they dispositively support either proposed definition. Rather, the claims generally speak of outputting or inputting data over a bus.

Infineon urges the court to consider the language of claim 26 of the '918 patent as illustrative of its view of the term:

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[9] The term "bus" is used in claims 1, 2, 6, 8, 16, 18, 19, 20, 24, 33, and 14 of the '918 patent, claims 1, 2, 4, 10, 15, 16, 18, and 25 of the '214 patent, claims 2, 14, 27, and 30 of the '263 patent and claim 26 of the '804 patent.

> 26. An integrated circuit device having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device outputs data on an external bus synchronously with respect to first and second external clock signals, the integrated circuit device comprises:
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> . . .
>
> interface circuitry, coupled to the external bus to receive a read request, the interface circuitry includes a plurality of output drivers, coupled to the external bus, to output data on the external bus in response to the internal clock signal, synchronously with respect to the first and second external clock signals and in accordance with the value stored in the first internal register.

'918 patent, Claim 26 (emphasis added). Infineon posits that this claim calls for data to be output onto the bus, and a read request to be received on the same bus, thus supporting its conclusion that "bus" means a multiplexed bus.[10] While the language of this single claim somewhat supports Infineon's construction, the specification must reviewed to determine how the inventors used the term "bus" and whether they intended the term to have a special meaning. See Watts v. XL Sys., Inc., 232 F.3d 877, 882 (Fed. Cir. 2000) ("One purpose for examining the specification is to determine if the patentee has limited the scope of the claims"). "[E]ven if [the claims] were clear on their face, [the court] must consult the

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[10] The testimony of Infineon's expert, Mr. Joseph McAlexander also supports this conclusion. See Markman Hearing, Tr. pg. 370 l. 13 to pg. 371, l. 19 (explaining that claim 1 of the '918 patent clearly indicates that a read request and output data are to travel across a single bus).

specification to determine if the patentee redefined any of those terms." Id. at 883.

2. The Specification

A close study of the patent specification reveals that, not only did the inventors act as their own lexicographers in defining the term "bus" to be the new inventive bus, but they also repeatedly explained how their various inventions worked in conjunction with the new bus, which they describe to be a centerpiece of the systems they claim to have invented.

The specification clearly and unambiguously describes the bus of the invention to be the inventive multiplexed bus. In the "Summary of Invention" the specification states:

> The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected in parallel to a bus where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

'918 patent, col. 3, ll. 50-60 (emphasis added). And again, later in the same section, the specification states, "In this system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data

over the same bus. Each memory device contains only a single bus interface with no other signal pins." '918 patent, col. 4, lines 9-13 (emphasis added). See also '918 patent col. 3, l. 61 through col. 4 l. 1. (the DRAM "is modified to use a wholly bus-based interface rather than the prior art combination of point-of-point and bus-based wiring used with conventional versions of these devices. The new bus includes clock signals, power and multiplexed address, data and control signals").

Throughout the "Detailed Description," the specification repeatedly explains the use of the new multiplexed bus:

> The present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system.
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> ***
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> The bus consists of a relatively small number of lines connected in parallel to each device on the bus. The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus. In many systems using the present invention, the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines.
>
> ***
>
> Virtually all the signals needed by the computer system can be sent over the bus.

'918 patent, col. 5, ll. 29-45 (emphasis added). The inescapable lesson that emerges from comparing the claims of the patents with the inventors' fulsome textual description of the invention is that the inventions include a new bus and new devices that work with the inventive bus, all to the inventor's stated purpose, which is "to provide a high speed multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system." '918 Patent, col. 5, ll. 29-33 (emphasis added).

Additionally, not only does the specification define "bus" to be a multiplexed bus, but it also sets a background for explaining how the inventive multiplexed bus works with various other features of Rambus' inventions. Thus, the explanation of the inventions also supports the conclusion that the term "bus" means the multiplexed bus. For example, every embodiment described in the specification involves the use of a multiplexed bus.[11] Not once do

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[11] See e.g. '918 patent, col. 4, ll. 1-4 ("In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bits wide.") (emphasis added); '918 patent, col. 5, ll. 59-64 ("In the preferred implementation, memory devices are provided that have no connections other than the bus connections described herein and CPUs are provided that use the bus of this invention as the principal, if not exclusive, connection to memory and to other devices on the bus.") (emphasis added); '918 patent, col. 8 ll. 17-25 ("The preferred bus architecture of this invention comprises 11 signals: BusData[0:7]; AddrValid; Clk1 and Clk2; plus an input reference level and power and ground lines connected in parallel to each device . . . . The bus lines for BusData[0:7] signals form a byte-wide, multiplexed data/address/control bus").

the patents indicate that any of the inventions can, or should be, used with the prior art dedicated bus architecture.

This understanding is confirmed by the testimony of Mr. Joseph McAlexander, Infineon's expert, who explains that the patents "describe several bus architectures. But in every instance when they describe the bus of the invention it is always a multiplexed address, data and control bus." Markman Hearing, Tr. p. 360, l. 25 to p. 361, l. 4. Rambus' expert did not refute this conclusion.

In Toro Co. v. White Consolidated Indus., Inc., 199 F.3d 1295 (Fed. Cir. 1999), the Federal Circuit found it significant that the disputed patent contained only one embodiment of the invention. On the issue of whether a "ring" described in the patent must be attached to the "cover," the court noted that:

> The specification and drawings show the restriction ring as 'part of' and permanently attached to the cover. No other structure is illustrated or described. . . .
>
> . . . This is not simply the preferred embodiment; it is the only embodiment. . . .
>
> . . . Nowhere in the specification, including its twenty-one drawings, is the cover shown without the restriction ring attached to it.

Id. at 1301. See also O.I. Corp. v. Tekmar Co. Inc., 115 F.3d 1576, 1581 (Fed. Cir. 1997) (rejecting patentee's argument that the invention could have smooth or cylindrical walls when "[a]ll of the 'passage' structures contemplated by the written description are thus either non-smooth or conical."); General Amer. Transp. Corp.

v. Cryo-Tran, Inc., 93 F.3d 766, 770 (Fed. Cir. 1996), cert. denied 520 U.S. 1155 (1997) (the disputed claim construction was "not just the preferred embodiment of the invention; it is the only one described. Nothing in the claim language, specification, or drawings suggests that any of the [limitations] may be eliminated . . ."") (emphasis in original). Likewise, it is significant here that Rambus does not list a single example of how any of the new inventions would work with any type of bus other than a multiplexed bus.[12]

The Federal Circuit's holding in Wang Labs., Inc. v. America Online, Inc., 197 F.3d 1377 (Fed. Cir. 1999) is instructive as well. In Wang, the court considered whether the ordinary and

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[12] The failure of the specification to describe any other kind of bus in connection with the invention distinguishes the principal decision upon which Rambus relies, Johnson Worldwide Assoc., Inc. v. Zebco Corp., 173 F.3d 985 (Fed. Cir. 1999). In Johnson Worldwide, the Federal Circuit placed great emphasis upon the fact that the disputed claims did not require the narrower construction. 175 F.3d at 991. The Johnson Worldwide opinion distinguished Laitram Corp. v. Morehouse Indus., Inc., 143 F.3d 1456 (Fed. Cir. 1998) (which adopted the narrower claim construction) because the written description in Laitram made clear that the asserted claims will bear only one interpretation. In Johnson Worldwide, there was no such unambiguous language in the claim; "nothing suggests that 'heading' is required to be the heading of a trolling motor." Johnson Worldwide, 175 F.3d at 991.

The facts of Johnson Worldwide are distinguishable from the Rambus patents here. The Johnson Worldwide court noted that the "many uses of the term throughout the . . . patent are consistent with a broader definition" and that the "[v]aried use of the term in the written description demonstrates the breadth of the term rather than providing a limited definition." Id. at 991. Thus, the dual usage of the term did not create "a special and particular definition" Id. Here, there are not varied uses of the term "bus," only a single multiplexed bus.

accustomed meaning of the term "frame" could be overridden by the inventor's explanation in the specification:

> The parties agreed before the district court that the term "frame" can in general usage be applied to bit-mapped display systems as well as to character-based systems . . . . The disagreement was as to whether the term "frame" in the '669 claims embraced this general usage, or whether the term would be understood by persons of skill in this field as limited to the character-based systems described in the '669 patent.

Wang, 197 F.3d at 1381. As is true here, the only system described and enabled in the specification and drawings in Wang used the narrower, specific arrangement of the character-based system. Id. at 1382. The only time that the patent mentioned non-character-based systems was in the "Background of Invention" section. Id. The Federal Circuit agreed with the district court's conclusion that those references were merely acknowledgments of the state of the prior art, not an enlargement of the patent's invention; and that a person skilled in the field of art would not have understood that those references were included in the applicant's invention. Id. Similarly, Rambus is limited to the description set forth in the specification, which is only a description of the multiplexed bus.

In an effort to distance the claims from the specification, Rambus argues that one skilled in the art would recognize that any kind of bus could be used with the many inventions of the specification, not just the new multiplexed bus. The Federal

Circuit has rejected this exact argument, which attempts to escape the language of the specification. See Watts, 232 F.3d at 883 (inventor's arguments that "one of ordinary skill would be aware of a myriad ways to effect a sealing connection . . . may be true, [but] it does not overcome the fact that the specification specifies that the invention uses misaligned taper angles"). The fact that the inventions might conceivably be used with any kind of bus does not overcome the oft-repeated assertions in the specification which describe, and even tout, the new Rambus inventive bus while demonstrating that the inventions are to be used with the multiplexed bus.

Rambus next argues that Infineon is trying to improperly limit the scope of the claim to the limitations described in the preferred embodiment. See Karlin Tech., Inc. v. Surgical Dynamics, Inc., 177 F.3d 968, 973 (Fed. Cir. 1999) ("The general rule, of course, is that the claims of a patent are not limited to the preferred embodiment, unless by their own language."); CVI/Beta Ventures, 112 F.3d at 1158 ("as a general matter, the claims of a patent are not limited by preferred embodiments"). The specification, however, clearly distinguishes between the "invention" of the multiplexed bus and "the preferred embodiment" of the bus. The patent often describes the broader invention of a bus multiplexed for address, data and control information. This description is then followed by a narrower description of the

'preferred embodiment' that is an implementation of the multiplexed bus.

For example, the patent states:

> The new bus includes clock signals, power and multiplexed address, data and control signals. In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bits wide. Persons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of the invention.

'918 patent, col. 3, l. 67 through col. 4, l. 7. (emphasis added). The new multiplexed bus is the broadly defined invention and the preferred embodiment has certain characteristics such as 8 or 16 mutliplexed lines, an AddressValid line, and addresses of up to 40 bits. Numerous references in the specification highlight these differences.[13] Usually, the preferred embodiments described in the

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[13] See e.g. 918 patent, col. 5, ll. 37-50 ("The bus carries substantially all address, data, and control information needed by devices for communication with other devices on the bus. . . . Using the organization described herein, very large addresses (40 bits in the preferred implementation) and large data blocks (1024 bytes) can be sent over a small number of bus lines 8 plus one control line in the preferred implementation).") ; '918 patent col. 14, ll. 49-67 ("In the bus-based system of this invention" a master can use the device ID to access a specific device "including the address and control registers. In the preferred embodiment, one master is assigned to carry out the entire system configuration process." (emphasis added); '918 patent, col. 16., ll. 12-21 ("The bus architecture of this invention can include more than one master device. The reset or initialization sequence should also include a determination of whether there are multiple masters on the bus, and if so to assign unique master ID numbers to each. Persons skilled in the art will recognize that there are many ways of doing this. For instance, the master could poll each device to determine

specification give a technical example of how the overall invention works, thus helping to explain the claim language. "Although claims are not necessarily restricted in scope to what is shown in a preferred embodiment, neither are the specifics of the preferred embodiment irrelevant to the correct meaning of claim limitations." Phonometrics, Inc. v. Northern Telecom, Inc., 133 F.3d 1459, 1466 (Fed. Cir. 1998). Where, as here, the several embodiments described in the specification each involves only a multiplexed bus, that weighs heavily in construing the term bus to mean a multiplexed bus. See Wang, 197 F.3d at 1383.

Finally, it is significant that the specification only mentions the generic (or "dedicated") bus architecture in the "Comparison of Prior Art" section.[14] In these references to "bus," however, the inventors are distinguishing their new inventive bus from the prior art. The inventors explain that "[n]one of the buses described in patents or other literature use only bused connections. All contain some point-to-point connections on the backplane." '918 Patent, col. 2, l. 67 to col. 3, l. 3. Thus, it

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what kind of device it is . . . .") (emphasis added).

[14] For example, the specification explains that the bus of an earlier patent (U.S. Patent No. 3,821,715) "multiplexes addresses and data over a 4-bit wide bus and uses point-to-point control signals to select particular RAMs or ROMs." 918 patent, col. 2 ll. 13-15. The specification also explains that in the DRAM of a previous patent (U.S. Patent 4,449,207) "[t]he external interface to this DRAM is convention, with separate control, address and data connections." '919 patent, col. 2, ll. 32-33.

does not help Rambus to point out, as it does, that this text of the comparison uses the same term ("bus") to describe a completely different architecture from the "new" bus which, according to Rambus, means that the term "bus" must necessarily encompass any set of information transfer lines, including those cited as prior art. The "Comparison With Prior Art" section states only what the invention does not cover; and, in so doing, the specification expressly distinguishes the prior art buses from the disclosed bus of the invention. Of course, it is settled that "[c]laims are not correctly construed to cover what was expressly disclaimed." Culter Corp. v. A.E. Staley Mfg. Co., 224 F.3d 1328, 1331 (Fed. Cir. 2000) (description in specification that distinguished other types of catalysts "effected a disclaimer of the other prior art acids"). See also Wang, 197 F.3d at 1382 (references to "bit-mapped" protocols in "Background of Invention" were acknowledgments of the state of the art and not an enlargement of the invention described in the patent). The argument which Rambus makes based on the term "bus" as used in the discussion of prior art runs afoul of this basic precept of claim construction.

In a further effort to use the discussions of prior art to support its proposed definition of "bus," Rambus relies on Clearstream Wastewater Sys. v. Hydro-Action, Inc., 206 F.3d 1440 (Fed. Cir. 2000), to argue that its inventions involve "combination

claims," therefore it is entirely permissible to include both the new and the generic buses in its inventions:

> In construing the disputed claim limitations, it must be kept in mind that the claims at issue in this case are combination claims. Combination claims can consist of new combinations of old elements or combinations of new and old elements. Because old elements are part of these combination claims, claim limitations may, and often do, read on prior art.

Id. at 1445 (internal citations omitted). Further, Clearstream explains that:

> Clearly, the written description does point out the disadvantages of the [prior art] rigid conduit system and the advantages of the [new] flexible-hose system. However, the written description does not require that only the new flexible-hose system, but not the old, rigid conduit system, could be used in the claimed wastewater treatment plant. It is well established in patent law that a claim may consist of all old elements . . . for it may be that the combination of old elements is novel and patentable. Similarly, it is well established that a claim may consist of all old elements and one new element, thereby being patentable.

Id. (emphasis added).

Infineon properly agrees that combination claims can include some, or even all, prior art elements. However, Infineon also is correct in asserting that the proper framework for the current analysis is whether one of ordinary skill in the art would understand the Rambus disclosure to assert the combination theory recently embraced by Rambus. The patent specification here does

not support that theory because, unlike Clearstream, the specification in Rambus' patents do not describe the generic prior art bus in combination with any of the claims. Indeed, the "Comparison With Prior Art" discussion is at considerable pain to dissociate the inventive bus, and its uses, from the prior art, and to establish a similar disconnect of the other inventions from the prior art. '918 Patent, col. 2, l. 7 to col. 3, l. 47.

Thus, the specification clearly demonstrates that when the inventors used the term "bus" in the claims, they were referring to the new multiplexed bus described in the specification.[15] Upon reading the patent, one skilled in the art would conclude that the patentee explicitly defined bus: "[t]he present invention includes a memory subsystem comprising at least two semiconductor devices . . . connected in parallel to a bus where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices." '918 patent, col. 3, ll. 50-55. Nothing in the specification - no drawing and no embodiment - indicates that the bus in the claims has the dictionary definition that Rambus now asserts.

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[15] Other than the "Comparison with Prior Art" section, the patent specification only once indicates that a bus can be anything but the multiplexed bus: "Persons skilled in the art recognize that certain devices, such as CPUs, may be connected to other signals lines and possibly to independent buses, for example a bus to an independent cache memory, in addition to the bus of this invention." '918 patent, col. 5, ll. 54-57. In this reference, the inventors clearly distinguish between the multiplexed bus of the invention and any other kind of bus to be used in the system.

3. The File History

Despite the obvious descriptions in, and implications of, the patent itself, Rambus argues that the patent history teaches that the term "bus" includes more than just the multiplexed bus. While it is doubtful that a court should look to the patent history to contradict the unambiguous meaning described in the specification, see Multiform Desiccants, 133 F.3d at 1478 ("[w]hen the specification explains and defines a term used in the claims, without ambiguity or incompleteness, there is no need to search further for the meaning of the term"), the patent history here does not in any fashion clarify the scope of the disputed term. Rambus relies upon two statements made, and actions taken, in the prosecution of the patents stemming from the 1990 '898 application.

In June 1997, during the prosecution of the parent application[16] to the '263 patent (which is also the grandparent to the '918 patent),[17] the Patent Examiner issued a requirement for

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[16] This application eventually issued as U.S. Patent No. 5,841,580.

[17] When considering a patent's prosecution history, it is proper to look to statements made in the prosecution of related patents stemming from the same application, as is the case here. See Elkay Mfg. Co. v. Ebco Mfg. Co., 192 F.3d 973, 980 (Fed. Cir. 1999) ("When multiple patents derive from the same initial application, the prosecution history regarding a claim limitation in any patent that has issued applies with equal force to subsequently issued patents that contain the same claim limitation."); Mark I Marketing Corp. v. R.R. Donnelley & Sons Co., 66 F.3d 285, 291 (Fed. Cir. 1995) ("Thus, the relevant prosecution history here includes not only the '659 application but also the parent '815 and grandparent '668 applications."); Jonsson v.

restriction under 35 U.S.C. § 121,[18] finding that this patent claimed two distinct inventions. The examiner divided the claims into two groups, one group describing a plurality of conductors to be used with the multiplexed bus and the second group describing an access-time register within the memory device (the latency invention).[19] Asserting that the groups were not "connected in

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Stanley Works, 903 F.2d 812, 818 (Fed. Cir. 1990) (prosecution history of parent application is relevant to understanding scope of claims issuing in a continuation-in-part application).

[18] A requirement for restriction is issued by the PTO when a patent application contains more than one distinctly claimed invention. 35 U.S.C. § 121.

[19] The June 9, 1997 Office Action explains:

> 4. Restriction to one of the following inventions is required under 35 U.S.C. 121:
>
> Group I. Claims 151-55, drawn to a memory device having a plurality of conductors being multiplexed for sequentially receiving an address, classified in Class 365, subclass 230.02.
>
> Group II. Claims 156-158, drawn to a semiconductor device having at least one access-time register, classified in Class 395, subclass 290.
>
> The inventions are distinct, each from the other because of the following reasons:
>
> 5. Inventions I and II are disclosed as different combinations which are not connected in design, operation or effect. These combinations are independent if it can be shown that (1) they are not disclosed as capable of use together, (2) they have different modes of operation, (3) they have different functions, or (4) they have different effects. (MPEP 806.04, MPEP 808.01). In the instant case the combinations

design, operation, or effect," the Patent Examiner required the inventors to elect to pursue only one group of claims. Rambus prosecuted the claims in Group II (the latency invention), resulting in the '580 patent.

From this action by the PTO and from the fact that the same Patent Examiner reviewed the '263 and '918 patents in suit, Rambus asks the Court to make the leap in logic that the PTO must have understood that the multiplexed bus was not necessary for every other invention arising from the specification. This kind of speculation into the motivations of the patent examiner is not useful to a reviewing court or a competitor reading the patent history. "It is the applicant's representations during the prosecution that potentially shed light on the construction of the claims." Laitram Corp. v. Morehouse Indus., Inc., 143 F.3d 1456, 1462-63 (Fed. Cir. 1998) (emphasis in original) (rejecting argument

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> [sic] the memory device in Group I does not require the access-time register of Group II, and the semiconductor device in Group II does not require the plurality of conductor being multiplexed to receive an address as claimed in Group I.
>
> 6. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for invention I is not required for invention II, restriction for examination purposes as indicated is proper.

(emphasis added).

that meaning could be derived from the representation of the reexamination requester). The snippet of patent history upon which Rambus relies only shows that: (a) a single Patent Examiner at one time indicated that some claims should not be lumped together, and (b) that, rather than making an affirmative response to this restriction, Rambus chose to drop the claims for the multiplexed bus and pursue the latency invention. No more can be inferred from this exchange.

Rambus also relies on a second piece of evidence contained in the file history. Specifically, in November 1995, a different Patent Examiner rejected claims pending in the grandparent to the '804 patent as being obvious in view of prior art reference, U.S. Patent No. 5,129,069 to Helm, et al. Under Rambus' view of the file history, the Patent Examiner must have equated the generic term "bus" (recited in claims 176-181 of the grandparent application) with the non-multiplexed bus contained in the Helm patent when he initially rejected the claims. Nevertheless, this same Patent Examiner allowed claim 26 of the '804 patent (which contains a reference to an external bus) to issue without requiring that the term "bus" be limited to a multiplexed bus. Again, this kind of guessing as to what a Patent Examiner may have been thinking is not generally helpful to construing the claim terms because it requires both the court and the public to pour over oftentimes complex and voluminous patent histories, speculate as to

the motivation behind an office action, and then follow the patents in an effort to divine whether that same Patent Examiner may have had reason to construe another claim in the same manner. This invitation to haphazard guesswork certainly cannot be considered sufficiently reliable to trump the clear language of the specification. See Vitronics, 90 F.3d at 1582 ("Usually, [the specification] is dispositive; it is the single best guide to the meaning of a disputed term").

Moreover, the standard for construing claims in the patent application process is far different than the standard for construing claims in a litigation context. Patent examiners construe claims under a broader standard than that used by a court in undertaking claim construction. The Federal Circuit has held that "[i]t would be inconsistent with the role assigned to the PTO in issuing a patent to require it to interpret claims in the same manner as judges who, post-issuance, operate under the assumption that the patent is valid." In re Morris, 127 F.3d 1048, 1054 (Fed. Cir. 1997). In the posture of a claim construction during litigation, if the intrinsic evidence is ambiguous, "another claim construction canon comes into play. Because the applicant has the burden to 'particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention' 35 U.S.C. § 112, ¶ 2 (1994), if the claim is susceptible to a broader and a narrower meaning, and the narrower one is clearly supported

by the intrinsic evidence while the broader one raises questions of enablement under § 112, ¶ 1, we will adopt the narrower of the two." Digital Biometrics, 149 F.3d at 1344. See also Athletic Alternatives, Inc. v. Prince Mfg. Inc., 73 F.3d 1573, 1581 (Fed. Cir. 1996) ("Were we to allow AAI successfully to assert the broader of the two senses of 'between' against Prince, we would undermine the fair notice function of the requirement that the patentee distinctly claim the subject matter disclosed in the patent from which he can exclude others temporarily.") Therefore, even if one were to conclude that the patent history casts doubt on the clear meaning of the specification (which it does not), Rambus should be limited to the embodiment and description of a multiplexed bus set forth in the specification because it is the narrower of the two constructions.

The simple fact here is that reference to the file history does not contradict the clarity given by the specification. What Rambus has done is fixate upon two isolated events in the file history and, without connecting them to the issued patents, urges the Court to ascribe significance to the events by divining what an examiner must have meant by directing a certain action. That kind of sophistry is not among the tools available for claim construction under the carefully defined protocol established for that task by the Federal Circuit.

4. Claim Differentiation

Rambus relies on the doctrine of claim differentiation to support its contention that "bus" means only a "generic" bus. The doctrine presumes "a difference in meaning and scope when different words or phrases are used in separate claims. To the extent that the absence of such difference in meaning and scope would make a claim superfluous, the doctrine of claim differentiation states the presumption that the difference between claims is significant." Toro Co., 199 F.3d at 1302 (Fed. Cir. 1999) (quoting Tandon Corp. v. United States Int'l Trade Comm'n, 831 F.2d 1017, 1023 (Fed. Cir. 1987)). Rambus highlights the claims contained in Rambus U.S. Patent No. 5,983,320 (the '320 patent),[20] in which the independent claims of the '320 patent cover the concept of the "new" multiplexed bus. Each claim contains qualifying language to limit the bus to one that carries multiplexed address, data and control information over the same bus. For example, claim 7 of that patent claims a method for programming memory having a bus, where the bus "compris[es] a group of general purpose signal lines carrying substantially all of the time-division multiplexed address, data and control information for a memory transaction, wherein the

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[20] The '320 patent is a "sister" or "brother" patent to the '804 patent. Rambus bases the notion of cross-patent claim differentiation on footnote 2 of Laitram Corp. v. Morehouse Indus., Inc., 143 F.3d 1456, 1460 n.2 (1998). Because the argument of claim differentiation fails for other reasons, it is assumed, without deciding, that this is a proper use of related patents and their prosecutions.

address information is indicative of a range of addresses for a corresponding one of the individually addressable discrete memory sections of the memory device . . ."[21] Therefore, Rambus argues that, when it wanted to limit the term "bus" to a bus that carries multiplexed information, it knew how to do so.

This argument is unavailing because it too contradicts the clear meaning of the specification. "The doctrine of claim differentiation cannot broaden claims beyond the scope that is supported by the specification." ATD Corp. v . Lydall, Inc., 159 F.3d 534, 541 (Fed. Cir. 1998). See also Multiform Desiccants, 133 F.3d at 1480 (same). "Although the doctrine of claim differentiation may at times be controlling, construction of claims is not based solely upon the language of other claims; the doctrine cannot alter a definition that is otherwise clear from the claim language, description, and prosecution history." O.I. Corp. v. Tekmar Co., Inc., 115 F.3d 1576, 1582 (Fed. Cir. 1997) (concluding "that the description provides a clear meaning for the language of the claim in this case and that it trumps the doctrine of claim differentiation"). See Toro Co., 199 F.3d at 1302 (claim differentiation "does not override clear statements of scope in the

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[21] According to Rambus, other Rambus patents include similar limiting language: U.S. Patent No. 5,995,443, Claim 33 ("the bus further includes a plurality of conductors terminated by an impedance to a power source") and U.S. Patent No. 6,032,215, Claims 33 and 37 (same) and Claim 38 ("the bus further includes a plurality of conductors wherein each conductor is terminated at an end by a resistor to a power terminal.")

specification and the prosecution history"). "The presumption that separate claims have different scope 'is a guide, not a rigid rule.'" ATD Corp., 159 F.3d at 541 (quoting Autogiro Co. of Am. v. United States, 384 F.2d 391, 404 (1967)). Having determined that the written specification limits the term "bus" to a multiplexed bus, it would be impermissible to allow Rambus to rely upon claim differentiation (citing to other patents) to broaden the meaning of the term.[22]

5. The Extrinsic Evidence

A review of the intrinsic evidence clearly demonstrates that when the term "bus" is used in the claims, it means the new inventive Rambus multiplexed bus. "Because the intrinsic record is

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[22] Along these same lines, Rambus argues that the claims of the original '898 application specifically claim a multiplexed bus, therefore the reasoning behind claim differentiation would apply to give "bus" a generic meaning within the specification because the original claims are part of the specification. See In re Dossel, 115 F.3d 942, 945 (Fed. Cir. 1997) ("The statute thus makes clear that under current law the specification of a patent consists of, and contains, both a written description of the invention and the claims."); Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 938 (Fed. Cir. 1990) ("The original claims as filed are part of the patent specification.") However, Dossel explains that "[m]odern usage . . . does not always conform to that statutory structure. For example, when discussing the process of claim construction, it is not uncommon for the process to be described as requiring an examination of the claims, the specification, and the prosecution history, treating them as distinct entities." 115 F.3d at 945. To the extent that the claims of the original application (which never issued), indicates that the inventors distinguished between the new multiplexed bus and a generic bus, this difference does not trump the clear descriptions in and implications of the written description.

clear, [the court] do[es] not give weight to an inconsistent dictionary definition," Digital Biometrics, 149 F.3d at 1346, as offered by Rambus.

A reading of the entire specification, without parsing it into individual quotes, unmistakably conveys that one of the primary benefits of every invention claimed in the patents in suit, and described in the specification, is to increase the speed of operation of the memory device. High speed access is the crown jewel of the specification and to that end, the multiplexed bus, in combination with the other inventions, increases the transfer speeds and decreases the amount of space occupied by the transfer lines. One skilled in the art reading the specification would certainly conclude that the "bus" meant to be used with the inventions is the new, inventive, high-speed, multiplexed bus. This conclusion is supported by the testimony of Joseph McAlexander, an expert who is experienced in the art and whose explanation for reaching that conclusion is highly credible because it is fully consonant with the specification and the claim language as explicated by the specification.[23] Mr. McAlexander's testimony

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[23] See Markman Hearing, Tr. p. 379, l. 20 to p. 380, l. 3 (Mr. McAlexander states, "Because the patent very strongly distinguishes numerous times the multiplex bus of the invention from the prior art, and states specifically in numbers of places, that the bus architecture of this new bus design is essential for the type of high speed activity that is required across the bus, and it distinguishes from the prior art because the prior art is stated not to be able to give that high speed type of transaction.")

is consistent with, and complimentary of, the intrinsic evidence.[24] On the other hand, the testimony of Rambus' expert, Dr. William Huber, is at odds with the intrinsic evidence and depends on a dictionary definition (other extrinsic evidence) that is not consistent with the many descriptions given by the inventors in the specification.

6. Construction

For the foregoing reasons, the term "bus" means a multiplexed set of signal lines used to transmit address, data and control information.

B. "Block Size Information"

In Rambus' invention, the user can specify the amount of data to be transferred over the bus during a bus transaction. This value is represented by the term "block size." The parties differ as to exactly how this value is to be measured. Rambus argues that "block size" is "the number of sequential data bits to be read from or written to the memory." In essence, Rambus reads block size to be a function of the number of sequential transactions on a bus necessary to respond to the transaction request. Infineon posits that "block size" "specifies the total amount of data that is to be

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[24] Other portions of Mr. McAlexander's testimony generally support this construction. See Markman Hearing, Tr., pg. 361, ll. 14-24; pg. 364, l. 22 to pg. 365, l.22; pg. 367, l. 17 to pg. 368, l. 13; pg. 371, ll. 3-19.

transferred on the bus in response to a transaction request." In other words, Infineon measures block size as a function of size or the amount of data to be transferred over the bus.

1. The Claim Language

The term "block size" occurs numerous times throughout the claims of the '918 patent and the '214 patent.[25] Most of the claims indicate that block size information defines the amount of data to be output or input by the memory device.[26] Indeed, there is nothing in the text of any claim which employs the term "block size" to indicate that "block size" means anything other than the amount of data to be transferred on the bus in response to some sort of transaction request. Thus, from reading the language of the claims, one skilled in the art would conclude that block size information is an instruction indicating the amount of data to be output (or input) by the memory device.

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[25] See claims 1, 2, 6, 9, 13, 15, 16, 18, 19, 20, 24, 29, 30, 31, 33, and 34 of the '918 patent and claims 1, 4, 6, 9, 10, 15, 16, 18, 21 and 25 of the '214 patent.

[26] See e.g. '918 patent, claim 1 ("first block size information defines a first amount of data to be output by the memory device. . . ."); '918 patent, claim 6 ("the memory device outputs the first amount of data corresponding to the first block size information. . . ."; '918 patent claim 13 ("the first block size information is a binary representation of the amount of data to be output after receipt of the first read request."); '214 patent, claim 1 ("first block size information defines a first amount of data to be output onto a bus. . . ."); '214 patent, claim 6 ("first block size information is a binary code indicative of the first amount of data to be output in response to the read request").

Rambus nonetheless urges that block size means "the number of sequential data bits to be read from or written to the memory" (presumably in response to a transaction request). Rambus does not identify any aspect of the claim language that would support its preferred definition. Additionally, it is worth noting that nothing in the claim language has been cited, or for that matter argued, as supporting the temporal or order requirements which would inhere in a sequential-based definition.

2. The Specification

In general terms, the specification explains that "[o]ne object of the present invention is to use a new bus interface built into semiconductor devices to support high-speed access to large blocks of data from a single memory device by an external user of the data, such as a microprocessor, in an efficient and cost-effective manner." '918 patent, col. 3, lines 21-25 (emphasis added). See also '918 patent, col. 4, lines 15-16 ("The bus supports large data block transfers . . .").

In discussing the preferred method of Device Address Mapping and the address registers therein employed, the specification explains that:

> The address registers can include a single pointer, usually pointing to a block of known size, a pointer and a fixed or variable block size value or two pointers, one pointing to the beginning and one to the end (or to the "top" and "bottom" of each memory block.

'918 Patent, col. 7, ll. 36-41. This text and that which follows it clearly bespeaks volume or amount as the measure of a block, not sequence or time.

The several other references to block size in the specification also teach that the term relates to amount of data not the order and timing of bits of data in a particular sequence.[27]

3. The Extrinsic Evidence

The construction offered by Rambus purports to be grounded in a table in column 11 of the specification. The table is in a section which refers to the preferred embodiment detailed in Figure 4 of the patent.[28] The specification states:

> BlockSize[0:3] specifies the size of the data block transfer. If BlockSize[0] is 0, the remaining bits are the binary representation of the block size (0-7). If BlockSize[0] is 1, then the remaining bits give the block size as a binary power of 2, from 8 to 1024. A zero-length block can be interpreted as a special command, for example, to refresh a DRAM without returning any data, or to change the DRAM from page mode to normal access mode or vice-versa.

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[27] '918 Patent, col. 11, ll. 1-5, ll. 41-48; col. 16, ll. 26-35, ll. 44-47; col. 17, ll. 1-2; col. 20, ll. 18-22.

[28] Figure 4 is replicated later in the Memorandum Opinion at II.C.2.

BlockSize[0:2]	Number of Bytes in Block
0–7	0–7 respectively
6	8
9	16
10	32
11	64
12	128
13	256
14	512
15	1024

Persons skilled in the art will recognize that other block size encoding schemes or values can be used.

'918 patent, col. 11, ll. 41-63.[29]

Rambus uses Table 11, as interpreted by its expert, Dr. Huber, as the basis for its construction that block size information is the number of sequential transfers necessary to carry the desired information over the bus line. The table is but one of many encoding schemes and does not purport to define or explain the meaning of block size generally. According to Dr. Huber, the block size indicated in the chart corresponds to the number of sequential transfers necessary to output the data onto the preferred embodiment 8-line bus. That is certainly not apparent from the patent document. Furthermore, during the Markman hearing, Dr. Huber connected almost all of his opinions, not to the patent specification, but rather to a prepared animation demonstrating how block size should be measured as sequential transfers of data. The reason for such reliance seems quite clear -- there simply is no

[29] During the Markman hearing, the parties agreed that the "6" contained in the second row of the chart is incorrect due to an apparent copying error. This number should be an "8."

support in the patent document. Also, that view is flatly contradicted by Infineon's expert who explained that block size contains information specifying the total amount of data that is to be transferred. See Markman Hearing, Tr. pg. 442, ll. 11-19. Mr. McAlexander has testified that "[t]he person of ordinary skill in the art would come to [the conclusion] that block size . . . means amount, and in just a plain, simple ordinary meaning of size is a[n] amount, it's not when or how." Markman Hearing, Tr. pg. 439, ll. 11-16 (testimony of Mr. McAlexander).

4. Construction

Infineon's construction is grounded in the specification and the claim language because both sources of information rather clearly reflect that block size is an amount of data, not the order in which it is delivered. There is nothing in the specification to support Rambus' somewhat contorted definition of block size. It simply defies reason (and the specification) to conceive of size as a measure of time.

Moreover, the construction urged by Rambus utterly ignores the clear language of the claim that block size is associated with a transaction request. (See, e.g., '918 Patent, Claim 1-7 and all other claims (8 through 38) dependent upon Claim 1-7). Infineon's definition encompasses this connection and, for that additional reason, it is the definition that is necessitated by the claim language and by the specification. Thus, "block size" is construed

to mean "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request."

C. "Read Request," "Write Request," and "Transaction Request"

The next three disputed terms are closely related, and, as the parties agree, it is appropriate to accord joint consideration. The purpose of memory devices (i.e., a DRAM) is to store data for later use. To this end, when a controller (or master) accesses the memory device to either store or retrieve data, it must send that device an instruction indicating what type of transaction is to be performed. At the most basic level, a read request is an instruction to the memory device to read data from the memory cells; a write request instructs the memory device to write data to the memory cells; and a transaction request instructs the memory device to perform some function, which could include reading or writing data. The controversy surrounding these terms involves whether these requests must contain not only the instruction of what action to perform (found in an "AccessType" field), but also must include address information indicating where in the memory cells the data should be read or written. Rambus contends that read, write and transaction requests contain only the instruction of what action to perform. For example, it proposes that read request be defined as "an instruction to read data from specified

memory cell(s) of the memory. This instruction is specified by a binary code[30] provided to the memory device during a single clock cycle and received by the memory device in response to a clock transition."

Infineon, on the other hand, argues that such requests must contain both the instruction of what kind of action to perform and address information indicating where that action is to occur on the memory device. Address information, containing both row and column identifiers, tells the memory device where the desired data is located (or to be located) within the plurality of the memory cells. In Infineon's construction, a "'read request' means 'a series of bits transmitted over the bus that contain multiplexed address and control information needed to request a read of data from a memory device.'" In addition to objecting to the failure of Rambus' definition to include address information, Infineon disagrees with the limitations inherent in Rambus' definition, specifically the requirements that the request be a "binary code," that it can be no longer than "a single clock cycle" of information, and that it must be "received in response to a clock transition." In its view, these limitations are not required by

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[30] Binary code, a term not in dispute here, is "a code that makes use of members of an alphabet containing exactly two characters, usually 0 and 1." *IEEE Standard Dictionary of Electrical and Electronics Terms*, 4th Ed., IEEE, Inc. NY, 4th Ed. Pg. 95.

the intrinsic evidence, and in some cases are actually inconsistent with the embodiments disclosed in the specification.

1. The Claim Language

Both parties agree that the terms "read request," "write request," and "transaction requests" are not terms of art and were used for the first time in the 1990 '898 application. Therefore, there is no ordinary and accustomed meaning for these terms. Some information, however, can be gleaned from the language of the claims.[31]

Infineon uses the language of claim 1 of the '918 patent, claim 1 of the '214 patent, claim 1 of the '263 patent and claim 26 of the '804 patent to demonstrate that all claims require that a device respond to 'read request':

> 1. A method of controlling a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:
>
> providing first block size information to the memory device, wherein the first block size information defines a first amount of data to

---

[31] The term "read request" occurs in claims 1, 6, 8, 13, 18, 19 24, 29, and 34 of the '918 patent; claims 1, 2, 6, 14, 15, 16, 18, and 29 of the '214 patent; claims 1, 2, 14, 24, 15, 27, and 30 of the '263 patent; and claim 26 of the '804 patent.

The term "write request" occurs in claims 2 and 20 of the '918 patent.

The term "transaction request" occurs in claims 18 and 25 of the '263 patent.

be output by the memory device onto a bus in response to a read request . . .

'918 patent, claim 1 (emphasis added).

1. A method of operating a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method comprising:

providing first block size information to the memory device, wherein the first block size information defines a first amount of data to be output onto a bus in response to a read request . . .

'214 patent, claim 1 (emphasis added).

1. A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:

a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request.

'263 patent, claim 1 (emphasis added).

26. An integrated circuit device having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device outputs data on an external bus synchronously with respect to first and second external clock signals, the integrated circuit device comprises:

a first internal register to store a value which is representative of a number of clock cycles to transpire before the integrated circuit device responds to a read request. . .

'804 patent, claim 26 (emphasis added).

The claims clearly so provide. Indeed, all but two of the disputed claims containing these terms[32] explicitly state that information is supplied "in response to" a read request, a write request or other transaction request. It is, of course, true, as Infineon contends, that, in order to "respond" to a request (i.e. outputting or inputting data), the desired response can only occur if the selected device is given the information necessary to generate that response. Because one of ordinary skill in the art would understand that both address and control information are required for the memory device to respond to a request, that request must contain more than just the binary code or "AccessType" suggested by Rambus. Given the nature of the information and the way the invention works, it seems self-evident from the claim language that a request is, as Infineon posits, a series of bits transmitted over the bus containing address and control information. This conclusion is further buttressed by the explanations of Mr. McAlexander. See Markman Hearing, Tr. pg. 417, ll. 18-25 ("certainly the read has to have some control. It tells you what kind of transaction is being requested. If the memory is to respond to that, it must know where to respond from, what

---

[32] Indeed, of those claims mentioning read request, write request and transaction request, only claims 14 and 29 of the '214 patent do not explicitly mention that the memory device is to respond to the read request and even those mention a read request in such a way as to indicate that the term means there what it means elsewhere (Claim 14 "before executing another read request"); (Claim 29 "after executing another read request.")

address"). Thus, the claim language, although not dispositive, strongly supports the view of read, write and transaction request taken by Infineon.

2. The Specification

Although not discussed as extensively as other terms, such as "bus," the terms here at issue are the subject of explication in the specification. For example, in the "Comparison With Prior Art" section, the inventors explain:

> Yet another object of this invention is to provide a method for transferring address, data and control information over a relatively narrow bus and to provide a method of bus arbitration when multiple devices seek to use the bus simultaneously.

'918 Patent, col. 3, ll. 35-39 (emphasis added). This statement of object remarks the key role of address, data and control information. And, as explained in the cited text, and above in construing the term "bus," the significance of the invention of the system is to accomplish quickly the commands necessary to initiate a request and secure a response.

Then, in the ensuing "Summary of Invention" discussion, the inventors say that "[i]n this system of the invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data over the same bus." '918 Patent, col. 4, ll. 9-11 (emphasis added). Though not explicitly mentioning a "request," this quote lends credence to the basic

notion that a memory device should receive both address and control information in order to be able to transmit or receive data.

Then, shortly thereafter, in describing a preferred implementation of the invention, the specification explains how a bus transaction is initiated "by sending a request packet (a sequence of bytes comprising address and control information)." '918 Patent, col. 6, ll. 60-63). This, too, teaches that a request (be it a read request, write request, or transaction request) includes the address and control information necessary to accomplish the request.[33]

Having established that the specification contemplates both address and control information are needed for a response, it is necessary to ascertain whether a read request should contain both categories of information. The definition which Rambus presses proposes that a transaction request would consist only of the "AccessType" found in the top row[34] of Figure 4, the preferred embodiment.

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[33] Again, this conclusion is supported by the expert testimony of Infineon's Mr. McAlexander. See Trans. pg. 417, lines 20-22 ("I found the control and address information were required in every instance that it was addressed in the specification").

[34] As shown in Figure 4, the rows represent time or clock cycles.

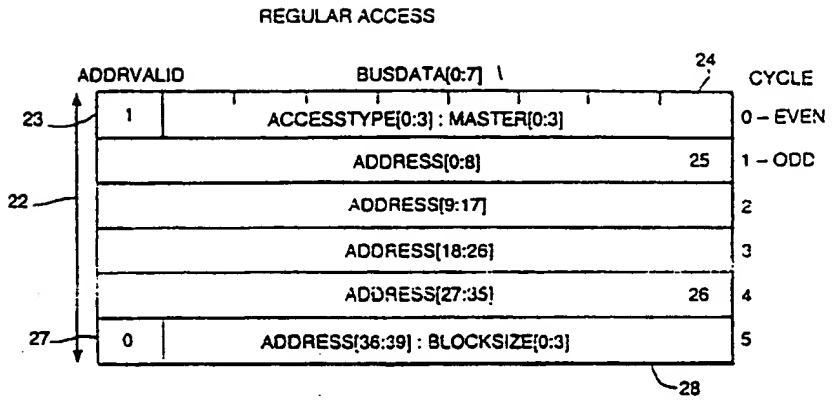

FIG_4

In the preferred embodiment, the AccessType instruction, which contains the control information specifying the type of request, would be a binary code 4-bits wide. The specification explains:

> The AccessType filed [sic: field] specifies whether the requested operation is a read or write . . . . In a preferred implementation, AccessType[0] is a Read/Write switch: if it is a 1, then the operation calls for a read from the slave (the slave to read the requested memory block and drive the memory contents onto the bus); if it is a 0, the operation calls for a write into the slave (the slave to read data from the bus and write it to memory).

'918 patent, col. 9, ll. 47-56. Rambus would limit the terms "read request," "write request" and transaction request" to only this AccessType field. In contrast, according to Infineon's interpretation, the requests must contain both the AccessType control information and the address information indicated on the remaining rows of Figure 4. To support its definition, Infineon points to the following passage from the specification:

> In a preferred implementation of the invention, to initiate a bus transfer over the bus, a master sends out a request packet, a contiguous series of bytes containing address and control information . . . .
>
> The device-selection function is handled using the bus data lines. AddrValid is driven, which instructs all slaves to decode the request packet address, determine whether they contain the requested address, and if they do, provide the data back to the master (in the case of a read request) or accept data from the master (in the case of a write request) in a data block transfer.

'918 patent, col. 8 l. 66 through col. 9, l. 4. The specification also explains that "[i]n some cases, a slave [memory device] may not be able to respond correctly to a request, e.g. for a read or write. In that situation, the slave should return an error message . . . or a retry message." '918 patent, col. 12, ll. 4-8. These references and others[35] illustrate that the memory should respond to the request. In order to respond, the memory device also must be given address information specifying where the data is to be read or written.

Additionally, though one must understand the technology to comprehend the import of the statement, the specification actually states that address rows are to be accessed during a request. The patent explains that the DRAM sense amps should be pre-charged and

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[35] See e.g. '918 patent, col. 8, ll. 48-49 ("a slave should preferable respond to a request in a specified time"); '918 patent, col. 8, ll. 24-29 ("AddrValid is used to indicate when the bus is holding a valid address request, and instructs a slave to decode the bus data as an address and, if the address is included on that slave, to handle the pending request."

"[t]his precharging allows access to a row in the RAM to begin as soon as the access request for either inputs (writes) or outputs (reads) is received and allows the column sense amps to sense data quickly." '918 Patent, col. 10, ll. 21-24 (emphasis added). Because one skilled in the art would recognize that "row" refers to a particular location on the plurality of memory cells, it follows that address information must be conveyed in order to access that row. That address information is contained in "the access request for either inputs (writes) or outputs (reads)."

Rambus definition would only indicate what type of operation to take place. See Markman Hearing, Tr. pg. 122, ll. 11-13 (testimony of Dr. Huber) ("We don't need the rest of the information [address information] to know that it's a read request"). The specification and the claims, however, clearly demonstrate the memory devices are not only to recognize the requested operation, but also respond to the request. Even Dr. Huber admitted that address information must be received for there to be a response. Dr. Huber took the view that this information could be conveyed at some other unspecified time. See Markman Hearing, Tr. pg. 141, ll. 20-22 (testimony of Dr. Huber). That approach is untenable because nowhere in the specification is it mentioned that address information should be sent at any other time than contemporaneous with the request.

Nor does the specification support the other foundational components of the narrow view of these terms expressed by Rambus. The construction urged by Rambus essentially attempts to equate the term "read request" with "AccessType," as shown in Figure 4, as the predicate for its requirement that "a read request" must be a binary code, occur in a single clock cycle, and be in response to a clock transition. The specification offers no warrant for such a limited construction, and, as Infineon points out, Rambus here is attempting artificially to limit the invention to the preferred embodiment of Figure 4, which describes a bus transaction that uses the preferred implementation of a 9-bit wide external bus. See '918 patent, col. 9, ll. 26-27 ("Each request packet uses all nine bits of the multiplexed data/address lines"). Because Figure 4 indicates that the AccessType is only 4-bits wide, it is possible for Rambus' proposed definition to occur in a single clock cycle. However, this requirement stems solely from Rambus' view that AccessType is a request. If a request contains both control and address information, then this would not be true. See Markman Hearing, Tr. pg. 431, ll. 8-12 (testimony of McAlexander) ("There is a specific control set of bits called the access type that does occur as a set of bits in a particular single cycle as shown in a preferred embodiment, but all that does is establish the type.") Similarly, there is nothing in the specification to support Rambus' requirement that the transaction request be received by the memory

device in response to a clock transition. See Markman Hearing, Tr. pg. 432, ll. 2-9 (testimony of McAlexander) (indicating that nothing in the specification supports this requirement).

Rambus contends that Infineon's construction incorrectly equates "read request" (or "write request" or "transaction request") with a request packet, arguing instead that a read request is actually a component of a request packet. For example, the specification states that "FIG. 4 shows the format of a request packet." '918 patent, col. 4, l. 66. It also explains that, in a preferred implementation, "a master sends out a request packet, a contiguous series of bytes containing address and control information." '918 patent, col. 8, ll. 60-63. The criticism is superficially appealing; however, the confusion results in large part from the fact that the specification uses the term "request" and "request packet" interchangeably. For example, the inventors explain, "FIG. 5 illustrates the format of a retry message 28 which is useful for read requests, . . . All DRAMs and masters can easily recognize such packet as an invalid request packet, and therefore a retry message." '918 patent, col. 12, ll. 33-39. See also '918 patent, col. 12, ll. 49-52 ("The master sends request packets and keeps track of periods when the bus will be busy in response to that packet. The master can schedule multiple requests so that the corresponding data block transfers do not overlap."; '918 patent, col. 12, ll. 58-61 ("Situations will arise, however,

where two or more masters send a request packet at or about the same time and the multiple requests must be detected. . . .) That drafting lapse is unfortunate, but it certainly is not dispositive because that text too must be interpreted in perspective of the whole specification.

Considering the claim language and the specification in its entirety and for the reasons explained above, the construction offered by Infineon is better supported by the patent document. Although that construction results in some overlap in the meanings of request and request packet, that overlap is inherent in the patent specification itself. Indeed, the most significant passage of the specification discussing read requests and write requests indicates that such a request is related to (if not synonymous with) a request packet: "AddrValid is driven, which instructs all slaves to decode the packet address determine whether they contain the requested address, and if they do, provide the data back to the master (in the case of read request) or accept data from the master (in the case of a write request) in a data block transfer." '918 Patent, col. 8, l. 66 through col. 9, l. 4 (emphasis added).

3. The File History

Those constructions derived from the claim language and specification are supported by the fact that, in the prosecution of the '804 patent, Rambus made statements to the PTO relating to the term "transaction request." In February 1999, Rambus submitted a

Preliminary Amendment in U.S. Patent App. 08/798,525 (issued as the '804 patent) in which it admitted that transaction requests are not simply a single clock-cycle access-time code. In response to a rejection by the Patent Examiner, Rambus stated that a "transaction request" contains identification information:

> When the identification information contained in the transaction request corresponds to the identification value stored in the internal register in a particular memory device on the module, that memory device executes the transaction request. Memory devices on the module having identification values which do not correspond to the identification information contained in the transaction request do not execute or respond to the request.

Supplemental Preliminary Amendment, U. S. Patent App. 08/798,525, p. 12 (emphasis added). Thus, Rambus explicitly represented that a transaction request contains more than just a binary code in the AccessType field: the above passage shows that device identification information also is contained in the transaction request. While this representation does not necessarily imply that Infineon's definition is unquestionably correct, it certainly undermines the construction now urged by Rambus.

4. Claim Differentiation

Claim 15 of the '214 patent refers to a "read request" without further limitation, while dependent claim 22 recites: "The method of claim 15 wherein the first block size information and the first read request are contained in a request packet." Rambus argues

that this language distinguishes a "read request" from a "request packet." As stated previously, the specification sometimes uses the terms "request" and a "request packet" interchangeably. Notwithstanding that drafting laxity, the differences in claim 15 and 22 do not refute the notion that a request contains address and control information. These claims simply add a third type of information, block size information, as a component of a request packet.

Given that the claim language clearly illustrates that a memory device is to respond to a read, write or transaction request and that Rambus has not explained how the device would respond without receiving address, data and control information, the claim language on its face supports the requirement that requests contain both address and control information. The specification, while not pellucid, also indicates that a request must contain such information so that it can respond to the request, whether the request be packetized or not. Rambus' narrow definition is not supported by the specification, and indeed, is refuted by the file history. Therefore, it is appropriate to conclude that "read request," "write request," and "transaction request" contain both address and control information indicating what type of transaction to perform and where the data should be located on the memory device.

5. Construction

For the foregoing reasons, the term "read request" is construed to mean "a series of bits transmitted over the bus that contain multiplexed address and control information needed to request a read of data from a memory device." The term "write request" is construed to mean "a series of bits transmitted over the bus that contain multiplexed address and control information needed to request a write of data to a memory device." The term "transaction request" is construed to mean "a series of bits transmitted over the bus that contain multiplexed address and control information needed to perform a transaction over the bus with a memory device."

D. "First and Second External Clock Signals"

The parties agree that the bus of the invention carries two external clock signals[36] which pace the exchange of information over the bus and provide timing synchronization for the memory system. The dispute arises over whether the second external clock signal must contain information that is different from the timing information sent by the first clock signal.

Although referred to as a "clock" by one skilled in the art, the clock of a memory chip is actually a set of timing information

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[36] As has been the convention of both the patent documents and the parties, the terms "clock signal" and "clock" are used interchangeably.

derived from an oscillating reference voltage ("V_{REF}") which cycles between two voltage levels. Rambus' proposed definitions do not require that the two signals contain different timing information, while Infineon's proposed definitions require that the second signal contain different information from the first.

1. The Claim Language

Every asserted claim in the '214 patent (the double data rate invention) and the '804 patent (the delayed lock loop invention) contains the terms "first external clock signal" and "second external clock signal."[37] Most of the claims simply indicate that data is to be output on the bus in response to the first and second external clock signals. Three claims, however, reveal that the two clock signals can be used by the memory device to create an internal clock:

> 25. The method of claim 15 further including generating at least one internal clock signal using the first and second external clock signals wherein the first amount of data corresponding to the first block size information is output onto the bus synchronously with respect to at least one internal clock signal.

'214 patent, claim 25.

> 26. The method of claim 25 further including generating a first internal clock signal using a delay locked loop and the first and second external clock signals.

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[37] See claims 1, 2, 4, 9, 10, 11, 15, 16, 18, 24, 25, and 26 of the '214 patent and claim 26 of the '804 patent.

'214 patent, claim 26.

> 26. An integrated circuit device having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device outputs data on an external bus synchronously with respect to first and second external clock signals, the integrated circuit device comprises:
>
> . . . .
>
> Delay locked loop circuitry to generate an internal clock signal using the first and second external clock signals . . . .

'804 patent, claim 26.

The claim language thus indicates that somehow the memory device is to use the information derived from the first and second clock signal to create in internal signal. One must consult the specification to understand how this is accomplished.

2. The Specification

In the "Background of the Invention" section, the specification relates that one "object of this invention is to provide a clocking scheme to permit high speed clock signals to be sent along the bus with minimal clock skew between devices." '918 patent, col. 3, ll. 27-29. "The two clocks together provide a synchronized high speed clock for all the devices on the bus." '918 patent, col. 8, ll. 29-30. Most significantly, in the "Clocking" subsection of the "Detailed Description," the inventors explain:

> Clocking a high speed bus accurately without introducing error due to propagation delays can be implemented by having each device monitor two bus clock signals and the[n] derive internally a device clock, the true system clock. The bus clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks.

'918 patent, col. 18, l. 63 through col. 19, l. 4. This idea of clock skew can be best understood by reference to Figures 8*a* and 8*b* of the specification.

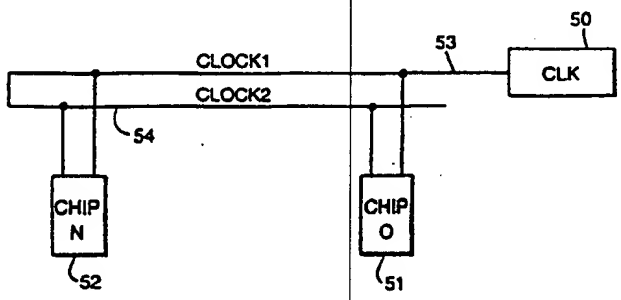

FIG_8A

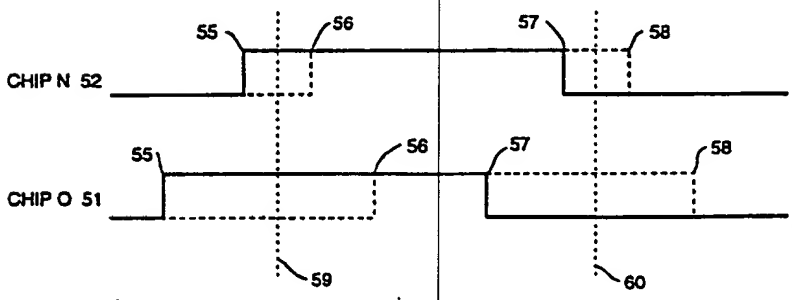

FIG_8B

The specification clearly demonstrates how these figures represent the two clock signals:

> Referring to FIG. 8*a*, in the preferred implementation, a bus clock generator 50 at one end of the bus propagates an early bus clock signal in one direction along the bus, for example on line 53 from right to left, to the far end of the bus. The same clock signal then is passed through the direct connection shown to a second line 54, and returns as a late bus clock signal along the bus from the far end to the origin, propagating from left to right. A single bus clock line can be used if it is left unterminated at the far end of the bus, allowing the early bus clock signal to reflect back along the same line as a late bus clock signal.
>
> FIG. 8*b* illustrates how each device 51, 52 receives each of the two bus clock signals at a different time (because of propagation delay along the wires), with constant midpoint in time between the two bus clocks along the bus. At each device 51, 52, the rising edge 55 of Clock1 53 is followed by the rising edge of 56 of Clock2 54. Similarly, the falling edge 57 of Clock1 53 is followed by the falling edge 58 of Clock2 54. This waveform relationship is observed at all other devices along the bus. Devices which are closer to the clock generator have a greater separation between Clock1 and Clock2 relative to devices farther from the generator because of the longer time required for each clock pulse to travers the bus and return along line 54, but the midpoint in time 59, 60 between corresponding rising of falling edges is fixed because, for any given device, the length of each clock line between the far end of the bus and that device is equal. Each device must sample the two bus clocks and generate its own internal device clock at the midpoint of the two.

'918 patent, col. 19, ll. 4-32. See also Fig. 13 of the '918 patent (showing how the rising and falling edges of the two bus clocks can be synchronized).

In essence, this portion of the specification explains how chips N and O, which are located in different positions along the bus lines, receive the clock signals at different points in time due to their locations relative to the origin of the clock signal. By reflecting the signal along a second line, the memory system can compensate for this delay and create a second clock signal. From these two signals, chips N and O create an internal clock signal which corrects the clock skew caused by propagation delay. In order to correct the skew, the two signals must necessarily contain different information, as Rambus' expert admitted. See Markman Hearing, Tr. pg. pp. 296-298 (testimony of Dr. Huber). Although the specification lists this clocking scheme as a preferred embodiment, it is actually the only embodiment of the clock in the entire specification. As with the analysis of the term "bus," it is significant that the specification limits the clock to a single embodiment. See generally Wang, 197 F.3d at 1380; Toro, 199 F.3d at 1301; O.I. Corp., 115 F.3d at 1581.

3. The Extrinsic Evidence

The constructions taught by the specification are confirmed by the testimony of Mr. McAlexander who explained that to one ordinarily skilled in the art that the Rambus clock scheme allows

the memory devices to sample each clock signal as it is received over the line and then averages the two signals such that every device is operating off the same clock, regardless of that device's location relative to the origin of the clock signal. Markman Hearing, Tr. pg. 457, line 2 to pg. 458, line 1 (testimony of Mr. McAlexander). Thus "the timing information and the difference between them is essential to this inventive concept of the clock design." Id.[38]

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[38] Mr. McAlexander's testimony also explains how the clocking scheme comes full circle to the primary objective of the invention and the use of a multiplexed bus:

> In the prior art where the address information goes down one bus and data is responded to the bus on a totally different bus - so you have a data bus that's separate and distinct from the address bus - you could send down the control [or] the address information to a chip, activate it, . . . it goes in, finds the data from the storage cells and immediately sends it out to the data bus which is a separate bus.
>
> In the multiplexed design, the data must share the same bus as the address information. And so the . . . controlling system must assure that at no time does address or control information reside on the bus at the same time that data . . . is coming back on the bus; otherwise, you would end up with a collision. . . .
>
> So in order to arbitrate that and to make sure that nothing is on the bus when it's not supposed to be, the whole system has to be in sync. Every system, every . . chip, every component on the bus has to be operating under the exact same timing constraints.
>
> That's why it's important and valuable . . . to use a clock design that will synchronize everything together.

In the interpretation of these terms, Rambus once again eschews the language of the specification, choosing to rely instead on the testimony of its expert who says that one skilled in the art would recognize that the first and second external clock signal can have, but does not need to have, different timing information in each signal. Therefore, according to Rambus, it is unnecessary to tie the claim definition to the language of the specification.[39] This approach runs afoul of the principle that the patent specification must always be reviewed to see if the patentee used the terms in a manner other than their ordinary meaning. Vitronics, 90 F.3d at 1582. Thus, even if one accepted Rambus' contention that the ordinary and accustomed meaning of first and external clock signals would be known to one of skill in the trade, the patent specification only describes a clocking scheme which corrects clock skew by creating an internal clock based on differing external clock signals.

4. Construction

Based on the claim language and the specification the term "first internal clock signal" is construed to mean "a periodic signal received by the memory device from an external source to

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Markman Hearing, Tr. pg. 465 l. 6 to pg. 466, l. 10.

[39] See Testimony of Dr. Huber, pg. 302, l. 25 - pg. 303 l. 2 ("I don't need to go to the patent to interpret the term. Clock signal is a well known term").

provide first timing information." The term "second internal clock signal" is construed to mean "a periodic signal received by the memory device from an external source to provide second timing information that is different from the first timing information."

E. Integrated Circuit Device

Lastly, the parties contest the meaning of "integrated circuit device" as that term is found in claim 26 of the '804 patent. Rambus contends that the term means a "circuit constructed on a single monolithic substrate, commonly called a 'chip.'" Infineon, however, argues that representations made in the prosecution of the '804 patent limit this term to "a device composed of integrated circuits that include at least an ID register and related interface and comparison circuitry."[40]

1. The Claim Language And The Specification

Neither the claim language nor the specification inform the present inquiry. Indeed, the specification mentions an integrated circuit only once.

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[40] The parties have agreed that "integrated circuit device" is only disputed as it occurs in claim 26 of the '804 patent and not as it appears in the other patents. This is because the relevant file history limits the representations made to the PTO to only the '804 patent.

2. The File History

The file history of this claim is the only relevant category of intrinsic evidence. During the prosecution of Claim 26 in the '804 patent, (which was at that time, U.S. Patent App. 08/798,525 or the '525 application) Rambus expressly limited its claims by adding certain restrictions in order to overcome the PTO's prior art rejections. In response to the rejections, Rambus submitted new claims -- including the claim that ultimately issued as claim 26 of the '804 patent. Rambus argued to the PTO that the newly submitted claims were different from prior art because they all contained a device ID register and relevant interface and comparison circuitry limitations:

> The new claims submitted in this Supplemental Preliminary Amendment have been added to more definitely and fully protect Applicants' invention. <u>These newly submitted claims are directed to a memory device (or an integrated circuit having memory) having (1) an internal register for storing an identification value, (2) interface circuitry to receive a request on an external bus, and (3) comparison circuitry to determine whether the identification information in the request corresponds to the identification value in the internal register</u> - wherein when the identification information corresponds to the identification value, the memory device responds to the request.

Supplemental Preliminary Amendment, U.S. Patent App. 08/798,525, pp. 11-12. The '804 patent issued subsequently. Thus, it appears that Rambus believed that its claims did not cover devices without a device ID register and relevant interface and comparison

circuitry. To allow Rambus to broaden its claim in the face of this restriction would defeat the public notice function of the patent history. In Hockerson-Halberstadt, Inc. v. Avia Group Intn'l, Inc., 222 F.3d 951 (Fed. Cir. 2000), the Federal Circuit explained:

> [The inventor's] argument therefore reduces to a request for a mulligan that would erase from the prosecution history the inventor's disavowal of a particular aspect of a claim term's meaning. Such an argument is inimical to the public notice function provided by the prosecution history. The prosecution history constitutes a public record of the patentee's representations concerning the scope and meaning of the claims, and competitors are entitled to rely on those representations when ascertaining the degree of lawful conduct, such as designing around the claimed invention. . . . Were we to accept [the inventor's] position, we would undercut the public's reliance on a statement that was in the public record and upon which reasonable competitors formed their business strategies.

Id. at 957 (internal citations omitted).

"Absent qualifying language in the remarks, arguments made to obtain the allowance of one claim are relevant to interpreting other claims in the same patent." Digital Biometrics, 149 F.3d at 1347. Rambus claims to have presented such "qualifying language" in a footnote of the above-quoted representation to the PTO, which mentions two of the inventive technologies claimed in this suit:

> The memory devices or integrated circuits having memory of the present invention may include additional and/or other inventive aspects, including, for example, delay lock loop circuitry and/or an internal register to

> store a value which is representative of a number of clock cycles to transpire before the memory device responds to a read request. This "latency" register may be employed to control the timing of the output data after receipt of, for example, a read request. However it is noted that, in light of the July 27, 1998 Office Action and the rejection based on Weymouth, these additional and/or other inventive aspects, although forming a basis of patentability in their own right, will not be the focus of these Remarks.

Supplemental Preliminary Amendment, Patent App. No. 08/798,525, p. 12, n. 1. Rambus maintains that the express exclusion of the delay locked loop system and the latency invention from the scope of the attorney's remarks makes it "preposterous" to read a device ID register limitation into the claims currently before the court. Instead, during the Markman hearing in this case, Rambus' expert Dr. Huber contended that the limitation applies to every other claim of the patent (claims 1-25) but not claim 26. This conclusion, according to Dr. Huber, is an obvious conclusion based on the fact that claim 26 includes the inventive technologies mentioned as additional and/or inventive features in the footnote.

Notwithstanding Rambus' current attempt to carefully craft its limitations without much support in the patent history, the footnote does not imply that the statement excludes claim 26, but rather establishes that, in addition to the device ID register, Rambus believed that it claims possessed other inventive features. The last sentence of the footnote shows that Rambus chose not to rely on those additional inventive features when distinguishing the

claims from prior art. See id. ("these additional and/or other inventive aspects, although forming a basis for patentability in their own rights, will not be the focus of these Remarks"). Therefore, it is appropriate to read "integrated circuit device" as containing a device ID register, interface circuitry to receive a request from an external bus, and comparison circuitry to determine whether the identification information in the request corresponds to the identification register of the device.

Moreover, Rambus' suggested requirement that the integrated device be constructed on a single monolithic substrate is not supported by the specification and actually is undermined by the doctrine of claim differentiation. Claim 182 of the Preliminary Amendment to Patent App. No. 08/222,646, claim 6 of Patent No. 5,638,334 and claim 18 of Patent No. 5,657,481 all included the limitation that the device was "on a single semiconductor substrate." Claim 26 of the 804 patent contains no such limiting language and the doctrine of claim limitation warns against reading such a limitation into the disputed claim language unless the intrinsic evidence counsels otherwise.

3. Construction

Thus, the patent history supports the construction that an integrated circuit device, as used on claim 26 of the '804 patent, must have a device ID register, interface circuitry and comparison circuitry.

III. The Extrinsic Evidence Generally: The Experts

The claim construction here has been accomplished largely without resort to extrinsic expert evidence, notwithstanding that the parties presented expert testimony addressing each disputed term. Having reviewed that testimony, the Court found it useful mostly in understanding the meaning of technical terminology other than the disputed terms as that terminology is used in the claims and specification. See Pitney Bowes, 182 F.3d at 1309 ("it is entirely appropriate, perhaps even preferable, for a court to consult trustworthy extrinsic evidence to ensure that claim construction it is tending to from the patent file is not inconsistent with clearly expressed, plainly apposite, and widely held understanding in the pertinent technical field").

As outlined in the substantive discussion of each term construed, Rambus pressed constructions that generally found little, if any, support in the claim language or the specification, depending in significant part upon the expert testimony of Dr. Huber whose testimony was generally at odds with the statements made by the inventors in the claims and specification. Thus, his extrinsic evidence had to be substantially disregarded as contradictory of the intrinsic evidence. Also, it was difficult to credit Dr. Huber's testimony on disputed terms because it reflected the general, and disturbing, tendency of Rambus to distance its current constructions from what the inventors said in making the

claims and explaining the inventions in the specification,[41] and, in so doing, to use the claim construction process to broaden claims, rather clearly not made in the intrinsic evidence.

The record here, and the approach to claim construction taken by Rambus, illustrate the wisdom and importance of the rules of law that establish a hierarchal distinction between intrinsic and extrinsic evidence. On the other hand, the testimony of Mr. Joseph McAlexander, the expert offered by Infineon, was quite helpful and very credible because it was tethered closely to the intrinsic evidence and was not contradictory of the claim language or the specification. Notwithstanding that his testimony was reliable and informative it was ultimately not essential except as specifically cited in the construction. See Pitney Bowes, 182 F.3d at 1309 ("Although the patent file may often be sufficient to permit the judge to interpret the technical aspects of the patent properly, consultation of extrinsic evidence is particularly appropriate to ensure that his or her understanding of the technical aspects of the patent is not entirely at variance with the understanding of one skilled in the art").

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[41] Moreover, Dr. Huber left the impression that he was more an advocate than he was one generally knowledgeable in the field of the invention, notwithstanding his rather impressive curriculum vitae.

CONCLUSION

For the foregoing reasons, the disputed terms in the four patents in suit are to be construed as reflected herein.